AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A fabrication method for a semiconductor CSP type package, comprising the steps of:

cutting a wafer on which LSI chips with LSI pads are formed to separate said LSI chips;

providing gaps around said LSI chips at equal intervals to array said LSI chips; ~~and~~

~~burying~~ filling said gaps with ~~an LSI chips~~ a chip layer insulative resin and allowing the resin to cure;

forming at least one wire layer electrically connected to the LSI pads and at least one wire layer resin;

forming CSP pads on the wire layer resin electrically connected to the at least one wire layer; and

slicing through the chip layer resin and the at least one wire layer resin to separate the LSI chips from one another to provide a plurality of the CSP packages;

wherein, in plan view of the CSP package:

a perimeter of the chip layer resin and wire layer resin lies entirely outside ~~to enlarge a wire forming area, thereby providing an external terminal mounting area extending farther outward from~~ a peripheral edge of ~~each of~~ said LSI

chip[[s]]; and

at least one of the CSP pads extends outside the peripheral edge of the LSI chip.

2. (currently amended) The fabrication method according to claim 1, wherein each of said LSI chips has an alignment mark for photolithography and said alignment mark is used to align patterning on said each LSI chip in said steps of forming said at least one wire layer ~~forming area~~ and said ~~external terminal mounting area~~ CSP pads.

3. (original) The fabrication method according to claim 1, wherein said LSI chips are only those chips which have been screened as good after separation.

4. (original) The fabrication method according to claim 2, wherein said LSI chips are only those chips which have been screened as good after separation.

5. (original) The fabrication method according to claim 1, wherein said LSI chips are adhered to a substrate with said gaps provided.

6. (original) The fabrication method according to claim 2, wherein said LSI chips are adhered to a substrate with

said gaps provided.

7. (currently amended) The fabrication method according to claim 1, wherein said gaps are provided by adhering said wafer to [[an]] a stretchable sheet, then cutting said wafer to separate said LSI chips and stretching said sheet isotropically.

8. (currently amended) The fabrication method according to claim 2, wherein said gaps are provided by adhering said wafer to [[an]] a stretchable sheet, then cutting said wafer to separate said LSI chips and stretching said sheet isotropically.

9. (new) A fabrication method for a semiconductor CSP type package, comprising the steps of:

cutting a wafer on which LSI chips with LSI pads are formed to separate said LSI chips;

separating the LSI chips from one another to provide gaps of predetermined width between adjacent said LSI chips;

filling said gaps with a chip layer resin and allowing the resin to cure;

forming at least one wiring layer electrically connected to the LSI pads and covering each said wiring layer with a wiring resin layer;

forming CSP pads on a topmost said wiring resin layer electrically connected to the at least one wiring layer; and

slicing through the cured chip layer resin and the at least one cured wiring resin layer to separate the LSI chips from one another to provide a plurality of the CSP packages;

wherein, in plan view of the CSP package:

a perimeter of the chip layer resin and each said wiring resin layer lies entirely outside a perimeter of said LSI chip; and

at least one of the CSP pads extends outside the peripheral edge of the LSI chip.

10. (new) A fabrication method for a semiconductor CSP type package, comprising the steps of:

attaching a wafer on which LSI chips with LSI pads are formed to a stretchable sheet;

cutting the wafer to separate said LSI chips;

stretching the sheet isotropically to separate the LSI chips from one another to provide gaps of predetermined width between adjacent said LSI chips;

with the LSI chips held in place, filling said gaps with a chip layer resin and allowing the resin to cure;

forming at least one wiring layer electrically connected to the LSI pads and covering each said wiring layer with a wiring resin layer;

forming CSP pads on a topmost said wiring resin layer electrically connected to the at least one wiring layer such that at least one of the CSP pads extends outside a peripheral edge of the LSI chip; and

slicing through the cured chip layer resin and the at least one cured wiring resin layer to separate the LSI chips from one another to provide a plurality of the CSP packages.